What is claimed is:

1. An image sensor comprising:

a plurality of image sensor pixels; and

a noise reduction circuit, receiving a first and second image part at a first time, and outputting a combination of said first and second image parts at said first time, and receiving said second image part along with a third image at a second subsequent time and outputting a combination of second and third image parts at said subsequent time.

2. A sensor as in claim 1 further comprising a fixed pattern noise reduction circuit, connected to receive said image parts, and to remove at least one amplifier offset therefrom.

3. A sensor as in claim 2 wherein said amplifier offset is an amplifier offsets from different rows of said column.

4. A sensor as in claim 1 further comprising at least one amplifier having an operational amplifier, a feedback capacitor connected across said operational amplifier, and a variable gain-setting capacitor at an input to said operational amplifier.

5. A sensor as in claim 1 wherein said noise reduction circuit includes a first passing transistor passing a reset level, a first capacitor storing said reset level, a second passing transistor passing a signal level, a second storage capacitor storing said signal level, and a crowbar circuit, operating to connect said first and second capacitors, to connect said signal level to said reset level to cause said first and second capacitors to equalize their charge.

6. A sensor as in claim 1, further comprising a controller, controlling said noise reduction circuit to obtain a value indicative of signal minus reset at a first time, and to obtain a value indicative of reset minus signal at a second time.

7. A sensor as in claim 6, wherein said noise reduction circuit includes a first sampling transistor sampling a reset value of the pixel, a second sampling transistor sampling a signal value of the pixel, and wherein said controller reverses an order of operating said transistor to change said sense.

8. A sensor as in claim 4, further comprising a reset transistor, coupled across said feedback capacitor, to reset a value of said feedback capacitor.

9. A sensor as in claim 1, wherein said noise reduction circuit includes a first fixed pattern noise reduction circuit, having first and second capacitor elements respectively storing signal and reset, a second fixed pattern noise reduction circuit having third and fourth capacitors respectively storing signal and reset for a second value, and outputting said first and second values at a first time, and outputting said second value along with a new third value at a second time to thereby re-use the second value at two different times.

10. A sensor as in claim 1, wherein said image sensor pixels are active pixels, each of which including a photoreceptor, and an in-pixel buffer transistor and an in-pixel selection transistor.

11. A method of binning pixels, comprising:

first obtaining a plurality n of pixels at a first time;

adding said n pixels together to provide a first n-binned signal;

obtaining another plurality n of pixels at a second time, wherein said another plurality of pixels includes n-1 of the same pixels as obtained in said first obtaining; and

binning said second pixels at said second time to produce a second n-binned signal different from the first n-binned pixel.

12. A method as in claim 11 wherein n=2.

13. A method as in claim 11 wherein n=3.

14. A method as in claim 11, further comprising removing pixel-to-pixel noise with a noise reduction circuit.

15. A method as in claim 14, further comprising using two separate noise reduction circuits, a first of which reduces offsets in a first pixel, a second of which reduces offsets in a second pixel, and said first and second pixels used to form said first n-binned signal, said second pixel value being retained for use with a third pixel later processed by said first noise reduction circuit to form said second n-binned signal.

16. A method as in claim 11, further comprising adding values of the pixels.

17. A method as in claim 16, wherein said adding comprises obtaining a first sensed pixel at a first time, obtaining a second sensed pixel at a second time, and adding the first and second sensed pixels.

18. A method as in claim 11, further comprising removing

offsets from amplifiers that amplify said pixels, prior to adding said pixels.

19. A binning sensor, comprising:

a plurality of pixels arranged in an array;

a configurable adder, selectively connected to add at least a plurality of pixel values to one another; and

an offset reduction circuit, removing certain amplifier offsets from said pixel values prior to said adding.

20. A sensor as in claim 19, wherein said offset reduction circuit includes first and second noise reduction circuit parts, each of a plurality of values in each noise reduction circuit part maintained for two cycles, and added to two different values.

21. A sensor as in claim 19, further comprising a first passing transistor operating to pass a reset level, a first reset holding capacitor holding said reset level, a second passing transistor operating to pass a signal level, and a second holding capacitor operating to store said signal level.

22. A sensor as in claim 21, further comprising a third passing transistor operating to selectively pass said reset level

from said first capacitor and a fourth passing transistor operating to selectively pass said signal level from said second holding capacitor.

23. A sensor as in claim 22, further comprising a controller, producing outputs which control said third and fourth transistors, said outputs controlled in a first direction to produce a first sense signal, and in a second direction to produce a second sense signal.